What is claimed is:

1. A method of assembling chips, comprising at least:

providing a first chip and a second chip;

forming at least one conductive pillar on the first chip;

forming at least a first conductive connecting material on said conductive pillar; and

performing a connecting process to electrically connect said first chip to the second chip via said first conductive connecting material.

2. The method according to Claim 1, further comprising forming a second conductive connecting material on said second chip, said second conductive connecting material physically and electrically connecting to said first conductive connecting material on said conductive pillar during said connecting process..

3.The method according to Claim 2, wherein the step of forming said second conductive connecting material comprises screen printing a paste-like conductive connecting material on said second chip.

4. The method according to Claim 2, wherein said connecting process comprises:

aligning and connecting said first conductive connecting material on said conductive pillar to said second conductive connecting material on said second chip; and

performing a reflow process.

5. The method according to Claim 1, wherein said conductive pillar is formed of a material selected from a group consisting of tin, lead, copper, nickel, silver, zinc, bismuth, magnesium, antimony, indium and an alloy of at least two thereof.

6. The method according to Claim 2, wherein said first conductive connecting material and said second conductive material are formed of a material selected from a group consisting of tin, lead, copper, nickel, silver, zinc, bismuth, magnesium, antimony, indium and an alloy of at least two thereof.

7. A method of assembling chips, comprising:

providing a first chip and a second chip;

forming at least one conductive pillar on the first chip;

forming at least one conductive connecting material on the second chip; and

performing a connecting process to electrically and physically connect said conductive pillar to said conductive connecting material.

8. The method according to Claim 7, wherein said step of forming at least one conductive connecting material comprises screen printing a paste-like conductive connecting material on said second chip.

9. The method according to Claim 7, wherein said connecting process comprises:

aligning and connecting said conductive pillar on said first chip to said conductive connecting material on said second chip;

performing a reflow process

10. The method according to Claim 7, wherein said conductive pillar is formed of a material selected from a group consisting of tin, lead, copper, nickel, silver, zinc, bismuth, magnesium, antimony, indium and an alloy of at least two thereof.

11. The method according to Claim 7, wherein said conductive connecting material is formed of a material selected from a group consisting of tin, lead, copper, silver, zinc, bismuth, magnesium, antimony, indium and an alloy of at least two thereof.

12. The method according to claim 7, wherein the conductive pillar and the conductive connecting material are formed of a material selected from a group consisting of tin, lead, copper, gold, silver, zinc, bismuth, magnesium, antimony, indium and an alloy of at least two thereof.

13. The method of Claim 7, wherein before the step of performing said connecting process, said conductive connecting material on said second chip comprises solder bumps.

14. The method of Claim 13, wherein said solder bumps have a bump height greater than 15 μm.

15. The method of Claim 7, wherein before the step of performing said connecting process, said conductive connecting material on said second chip comprises solder balls.

16. The method of Claim 15, wherein said solder balls have a ball height greater than 15 μm.

17. A multi-chip structure comprising:

a first chip;

a second chip;

at least a conductive pillar on the first chip; and

a conductive connecting material connecting said conductive pillar to said second chip.

18. The structure of Claim 17, wherein the melting point of said conductive pillar is higher than the fusion temperature of said conductive connecting material.

19. The structure of Claim 17, wherein said conductive pillar is formed of a material selected from a group consisting of tin, lead, copper, nickel, silver, zinc, bismuth, magnesium, antimony, indium and an alloy of at least two thereof.

20. The structure of Claim 17, wherein said conductive connecting material is formed of a material selected from a group consisting of tin, lead, copper, nickel, silver, zinc, bismuth, magnesium, antimony, indium and an alloy of at least two thereof.

21. A multi-chip module, comprising:

a carrier;

a first chip mounted on and electrically connected to said carrier;

a second chip;

a plurality of conductive pillars on the first chip; and

a conductive connecting material connecting the conductive pillars to the second chip.

22. The module of Claim 21, wherein said first chip comprises an active surface, on which said conductive pillar is formed, and a rear surface attached to the carrier.

23. The module of Claim 21, wherein said first chip further comprises at least one wire-bonding pad at peripheral area not blocked by said second chip and said wire-bonding pad is electrically connected to said carrier through at least one bonding wire.

24. The module of Claim 21, wherein said carrier is a substrate or a lead frame.

25. The module of Claim 24, wherein said substrate is an organic, glass, ceramic or metal substrate.

26. The module of Claim 21, wherein said carrier further comprises an opening perforating therethrough to accommodate said second chip therein.

27. The module of Claim 21, wherein said fist chip further comprises a plurality of solder bumps at peripheral area not blocked by said second chip and said solder bumps are electrically connected to said carrier.

28. The module of Claim 21, further comprising an encapsulate material in the gap between said first and said second chip and encapsulating the electrically connection portion between said first chip and said carrier.

29. A method of assembling carriers, comprising:

providing a first carrier and a second carrier;

forming at least one first conductive pillar on said first carrier;

forming at least one second conductive pillar on said second carrier;

forming at least one conductive connecting material on said second conductive pillar; and

performing a fusion process to electrically connect said first and said second conductive pillars via said conductive connecting material.

30. The method according to Claim 29, wherein said first conductive pillar has a melting temperature higher than the fusion temperature of said conductive connecting material and said second conductive pillar has a melting temperature higher than the fusion temperature of said conductive connecting material.

31. The method according to Claim 29, wherein said first conductive pillar and said second pillar have a cross section with the same shape and dimension.

32. The method according to Claim 29, wherein said first conductive pillar and said second pillar have a cross section with the substantially similar shape and substantially close dimension.

33. The method according to Claim 32, wherein said substantially close dimension is within 10 μm per side.

34. The method according to Claim 29, wherein said first conductive pillar has a height greater than that of said second conductive pillar and the height of said second conductive pillar is smaller than 25 μm.

35. The method according to Claim 29, wherein said first carrier is a chip, a substrate or a ceramic substrate.

36. The method according to Claim 29, wherein said second carrier is a chip, a substrate or a ceramic substrate.

37. An assembly structure of carriers, comprising:

a first carrier;

a second carrier;

at least one first conductive pillar positioned on said first carrier and between said first and said second carriers;

at least one second conductive pillar positioned on said second carrier and between said first and said second carriers; and

a conductive connecting material connecting said first and said second conductive pillars.

38. The structure of Claim 37, wherein the melting point of said first conductive pillar is higher than the fusion temperature of said conductive connecting material and the melting point of said second conductive pillar is higher than the fusion temperature of said conductive connecting material.

39. The structure of Claim 37, wherein said first conductive pillar and said second pillar have a cross section with the same shape and dimension.

40. The structure of Claim 37, wherein said first conductive pillar and said second pillar having a cross section with the substantially similar shape and substantially close dimension.

41. The structure of Claim 37, wherein said substantially close dimension is within 10 μm per side.

. 42. The structure of Claim 37, wherein said first conductive pillar has a height greater than that of said second conductive pillar and the height of said second conductive pillar is smaller than 25 μm.

. 43. The structure of Claim 37, wherein said first carrier is a chip, a substrate or a ceramic substrate.

44. The structure of Claim 37, wherein said second carrier is a chip, a substrate or a ceramic substrate.

45. An multi-chip structure, comprising:

a first chip comprising:

a plurality of electronic devices;

at least a fine-line interconnection layer over the electronic devices and electrically and physically connected with the electronic devices;

a passivation layer over the fine-line interconnection layer having a plurality of openings;

a plurality of original pads in the openings of said passivation layer;

a post-passivation metal scheme over said passivation layer, wherein said post-passivation metal scheme comprises at least a gold

layer with an underlying adhesion/barrier layer, said gold layer has a thickness larger than 1 μm, the post-passivation metal scheme comprises a plurality of wire-bonding pads, a plurality of bump pads and a plurality of redistribution lines, the wire-bonding pads and the bump pads are defined at certain locations of a surface of said gold layer, and the redistribution lines connects the bump pads or the wire-bonding pads to the original pads; and

a first conductive connecting material overlaying said bump pads;

a second chip mounted over said first chip, wherein said second chip has a plurality of metal contacts; and

a second conductive connecting material connecting said metal contacts and said first conductive connecting material to electrically connect said first chip and said second chip.

46. The structure of Claim 45, wherein the first chip further comprises an under-bump-metallurgy layer between said first conductive connecting material and said bump pads

47. The structure of Claim 46, wherein said under-bump-metallurgy layer comprises a titanium layer, a copper layer and a nickel layer, from said bump pads side up sequentially.

48. The structure of Claim 46, wherein said under-bump-metallurgy layer comprises a titanium-tungsten-alloy layer, a copper layer and a nickel layer, from said bump pads side up sequentially.

49. The structure of Claim 46, wherein said under-bump-metallurgy layer comprises a chromium layer, a copper layer and a nickel layer, from said bump pads side up sequentially.

50. The structure according of Claim 45, wherein said first conductive connecting material is formed from material comprising a high lead solder, a tin-lead alloy, a tin-silver alloy, a tin-silver-copper alloy, a tin-bismuth alloy, a tin-silver-indium alloy, a tin-bismuth-zinc alloy, a tin-zinc alloy, a tin-bismuth-silver-copper alloy, a tin-silver-copper-antimony alloy, a tin-antimony alloy or a tin-zinc-indium-silver alloy.

51. The structure of Claim 45, wherein said second conductive connecting material comprises a tin-lead alloy, a tin-silver alloy, a tin-silver-copper alloy, a tin-bismuth alloy, a tin-silver-indium alloy, a tin-bismuth-zinc alloy, a tin-zinc alloy, a tin-bismuth-silver-copper alloy, a tin-silver-copper-antimony alloy, a tin-antimony alloy or a tin-zinc-indium-silver alloy.

52. The structure of Claim 45, wherein said post-passivation metal scheme further comprises at least one metal layer between said gold layer and said passivation layer, with at least one polymer layer between said gold layer and said metal layer or between the metal layers.

53. The structure of Claim 52, wherein said polymer layer is made of polyimide, benzocyclobutene, porous dielectric material, parylene, or elastomer.

54. The structure of Claim 45, wherein said post-passivation metal scheme is covered with a polymer layer, with the said wirebonding pads and said bump pads exposed.

55. The structure of Claim 54, wherein said polymer layer is made of polyimide, benzocyclobutene, solder mask material, porous dielectric material, parylene, or elastomer.

56. The structure of Claim 45, further comprising a polymer layer between said passivation layer and said post-passivation metal scheme..

57. The structure of Claim 56, wherein said polymer layer is made of polyimide, benzocyclobutene, porous dielectric material, parylene, or elastomer.

58. The structure of Claim 45, wherein said adhesion/barrier layer comprises a titanium-tungsten alloy, titanium, titanium-nitride or tantalum-nitride.

59. The structure of Claim 45, wherein said first conductive connecting material is pad-shaped.

60. The structure of Claim 59, wherein said first conductive connecting material has a height larger than 3 μm.

61. The structure of Claim 45, wherein said second conductive connecting material is pad-shaped.

62. The structure of Claim 61, wherein said second conductive connecting material has a height larger than 3 μm.

63. A method for fabricating a multi-chip structure, comprising:

providing a first chip comprising:

a plurality of electronic devices;

at least a fine-line interconnection layer over the electronic devices and electrically and physically connected with the electronic devices;

a passivation layer over the fine-line interconnection layer having a plurality of openings;

a plurality of original pads in the openings of said passivation layer; and

a post-passivation metal scheme over said passivation layer, wherein said post-passivation metal scheme comprises at least a gold layer with an underlying adhesion/barrier layer, said gold layer has a thickness larger than 1 μm, the post-passivation metal scheme comprises a plurality of wire-bonding pads, a plurality of bump pads and a plurality of redistribution lines, the wire-bonding pads and the bump pads are defined at certain locations of a surface of said gold layer, and the redistribution lines connects the bump pads or the wire-bonding pads to the original pads;

providing a second chip mounted over said first chip, wherein said second chip has a plurality of metal contacts;

forming a first conductive connecting material overlaying said bump pads;

forming a second conductive connecting material overlaying said metal contacts;

performing a connecting process to electrically and physically connect the first conductive connecting material and the second conductive connecting material.

64. The method of Claim 63, wherein said gold layer is formed by electroplating.

65. The method of Claim 63, wherein said first conductive connecting material is pad-shaped.

66. The method of Claim 65, wherein said first conductive connecting material has a height larger than 3 μm.

67. The method of Claim 63, wherein said first conductive connecting material is ball-shaped.

68. The method of Claim 67, wherein said first conductive connecting material has a height larger than 15 μm.

69. The method of Claim 63, wherein said second conductive connecting material is pad-shaped.

70. The method of Claim 69, wherein said second conductive connecting material has a height larger than 3 μm.

71. The method of Claim 63, wherein said second conductive connecting material is ball-shaped.

72. The method of Claim 71, wherein said second conductive connecting material has a height larger than 15 μm.

73. The method of Claim 63, wherein said first conductive connecting material is formed from material comprising a high lead solder, a tin-lead alloy, a tin-silver alloy, a tin-silver-copper alloy, a tin-bismuth alloy, a tin-silver-indium alloy, a tin-bismuth-zinc alloy, a tin-zinc alloy, a tin-bismuth-silver-copper alloy, a tin-silver-copper-antimony alloy, a tin-antimony alloy or a tin-zinc-indium-silver alloy.

74. The method of Claim 63, wherein said second conductive connecting material comprises a tin-lead alloy, a tin-silver alloy, a tin-silver-copper alloy, a tin-bismuth alloy, a tin-silver-indium alloy, a tin-bismuth-zinc alloy, a tin-zinc alloy, a tin-bismuth-silver-copper alloy, a tin-silver-copper-antimony alloy, a tin-antimony alloy or a tin-zinc-indium-silver alloy.